Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A0**
2. **A1**
3. **A2**
4. **N. E1**
5. **N. E2**
6. **N. E3**
7. **N. 07**
8. **GND**
9. **N. 06**
10. **N. 05**
11. **N. 04**
12. **N. 03**
13. **N. 02**
14. **N. 01**
15. **N. 00**
16. **VCC**

**.062”**

**.096”**

**1 16 16 15**

**14**

**13**

**12**

**11**

**8 8 9 10**

**2**

**3**

**4**

**5**

**6**

**7**

**ACT138T**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: ACT138T**

**APPROVED BY: DK DIE SIZE .062” X .096” DATE: 3/14/17**

**MFG: TEXAS INSTRUMENTS THICKNESS .011” P/N: 54ACT138**

**DG 10.1.2**

#### Rev B, 7/19/02